COMPUTER PROCESSING ARCHITECTURE HAVING A SCALABLE NUMBER OF PROCESSING PATHS AND PIPELINES

ABSTRACT OF THE DISCLOSURE

A processing core comprising R-number of processing pipelines each comprising N-number of processing paths. Each of the R-number of processing pipelines are synchronized together to operate as a single very long instruction word (VLIW) processing core. The VLIW processing core is configured to process R x N-number of VLIW sub-instructions in parallel. In addition, the R-number of pipelines can be configured to operate independently as separately operating pipelines. In accordance with one embodiment of the present invention, each of the R-number of processing pipelines comprises S-number of register files, such that the processing core comprises R x S-number of register files. In accordance with another embodiment of the present invention, each of the R-number of processing pipelines comprises one register file for every two of the N-number of processing paths, such that S = N/2. In accordance with yet another embodiment of the invention, a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together.